FAIRCHILD SEMICONDUCTOR™

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# 74LVQ74
# Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

## General Description

The LVQ74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level

LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

## Features

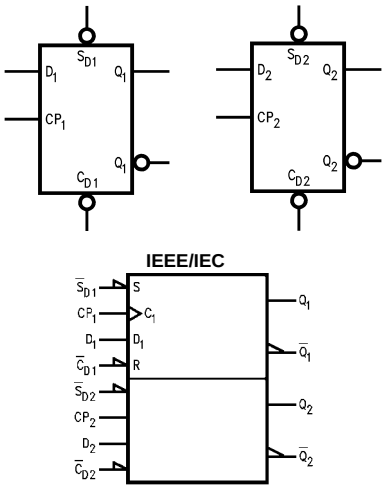
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

## Ordering Code:

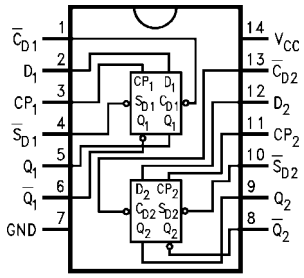
| Order Number | Package Number | Package Description |
|---|---|---|
| 74LVQ74SC | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74LVQ74SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Logic Symbols




## Connection Diagram



## Pin Descriptions

| Pin Names | Description |
|---|---|
| $D_1$, $D_2$ | Data Inputs |
| $CP_1$, $CP_2$ | Clock Pulse Inputs |
| $\overline{C}_{D1}$, $\overline{C}_{D2}$ | Direct Clear Inputs |
| $\overline{S}_{D1}$, $\overline{S}_{D2}$ | Direct Set Inputs |
| $Q_1$, $\overline{Q}_1$, $Q_2$, $\overline{Q}_2$ | Outputs |

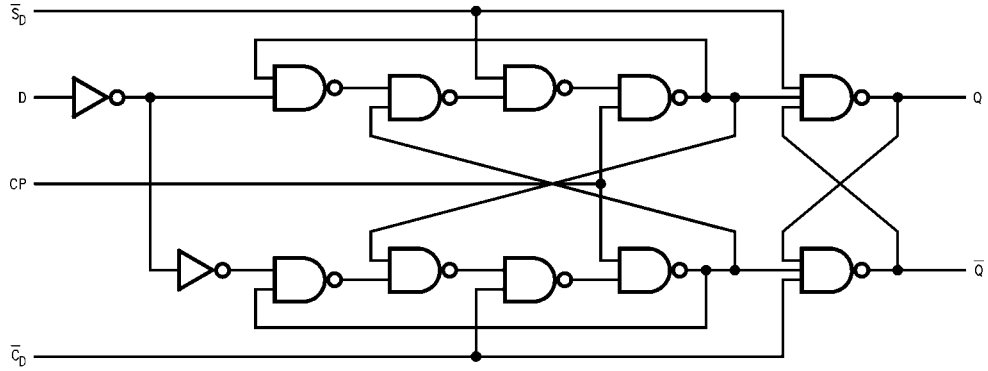
 

## Truth Table

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| $\overline{S}_D$ | $\overline{C}_D$ | CP | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | ⌐ | H | H | L |
| H | H | ⌐ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
$Q_0(\overline{Q}_0)$ = Previous Q($\overline{Q}$) before LOW-to-HIGH Transition of Clock

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current ($I_{CC}$ or $I_{GND}$) | ±200 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| DC Latch-Up Source or Sink Current | ±100 mA |

## Recommended Operating Conditions (Note 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 2.0V to 3.6V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate (ΔV/Δt) | |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 3.0V | 125 mV/ns |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = +25°C | $T_A$ = −40°C to +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum High Level | 3.0 | 1.5 | 2.0 | 2.0 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 3.0 | 1.5 | 0.8 | 0.8 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| $V_{OH}$ | Minimum High Level Output Voltage | 3.0 | 2.99 | 2.9 | 2.9 | V | $I_{OUT}$ = −50 μA |
| | | 3.0 | | 2.58 | 2.48 | V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ (Note 3) $I_{OH}$ = −12 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 3.0 | 0.002 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 μA |
| | | 3.0 | | 0.36 | 0.44 | V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ (Note 3) $I_{OL}$ = 12 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 3.6 | | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OLD}$ | Minimum Dynamic Output Current (Note 4) | 3.6 | | | 36 | mA | $V_{OLD}$ = 0.8V Max (Note 5) |
| $I_{OHD}$ | | 3.6 | | | −25 | mA | $V_{OHD}$ = 2.0V Min (Note 5) |
| $I_{CC}$ | Maximum Quiescent Supply Current | 3.6 | | 2.0 | 20.0 | μA | $V_{IN}$ = $V_{CC}$ or GND |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 3.3 | 0.2 | 0.8 | | V | (Note 6)(Note 7) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 3.3 | −0.2 | −0.8 | | V | (Note 6)(Note 7) |
| $V_{IHD}$ | Maximum High Level Dynamic Input Voltage | 3.3 | 1.7 | 2.0 | | V | (Note 6)(Note 8) |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | 3.3 | 1.6 | 0.8 | | V | (Note 6)(Note 8) |

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 6:** Worst case package.

**Note 7:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 8:** Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$), f = 1 MHz.

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | 2.7 | 50 | 100 | | 40 | | MHz |
| | | $3.3 \pm 0.3$ | 100 | 125 | | 95 | | |
| $t_{PLH}$ | Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ | 2.7 | 3.5 | 9.6 | 16.9 | 3.5 | 19.0 | ns |
| | | $3.3 \pm 0.3$ | 3.5 | 8.0 | 12.0 | 2.5 | 13.0 | |
| $t_{PHL}$ | Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ | 2.7 | 4.0 | 12.6 | 16.9 | 3.5 | 19.0 | ns |
| | | $3.3 \pm 0.3$ | 4.0 | 10.5 | 12.0 | 3.5 | 13.5 | |
| $t_{PLH}$ | Propagation Delay $CP_n$ to $Q_n$ or $\overline{Q}_n$ | 2.7 | 4.5 | 9.6 | 19.0 | 4.0 | 23.0 | ns |
| | | $3.3 \pm 0.3$ | 4.5 | 8.0 | 13.5 | 4.0 | 16.0 | |
| $t_{PHL}$ | Propagation Delay $CP_n$ to $Q_n$ or $\overline{Q}_n$ | 2.7 | 3.5 | 9.6 | 19.7 | 3.5 | 21.0 | ns |
| | | $3.3 \pm 0.3$ | 3.5 | 8.0 | 14.0 | 3.5 | 14.5 | |
| $t_{OSHL}$ | Output to Output Skew (Note 9) | 2.7 | | 1.0 | 1.5 | | 1.5 | ns |
| $t_{OSLH}$ | Data to Output | $3.3 \pm 0.3$ | | 1.0 | 1.5 | | 1.5 | |

**Note 9:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$). Parameter guaranteed by design.

## AC Operating Requirements

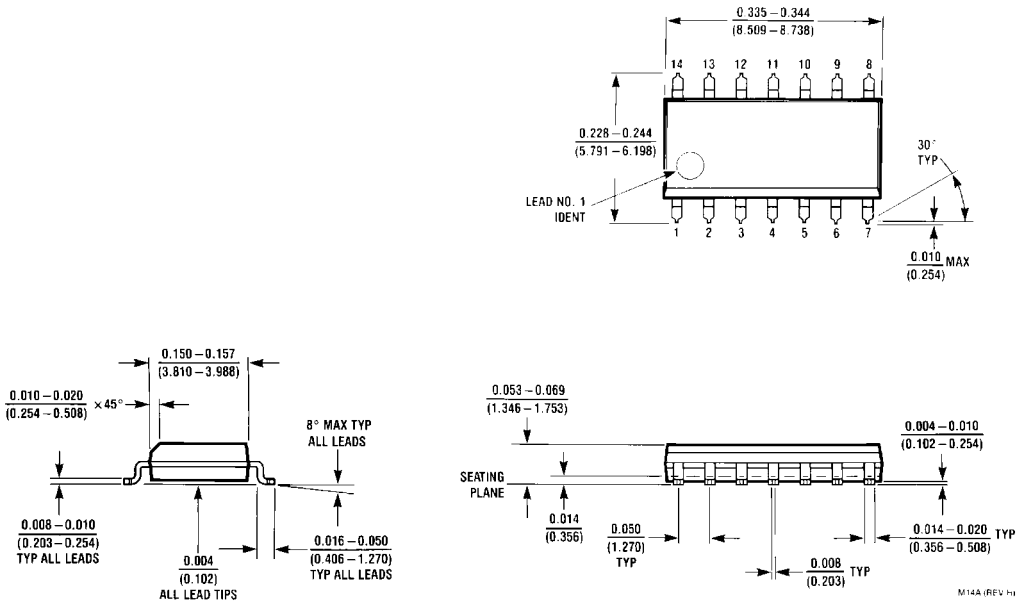
| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$, $C_L = 50$ pF | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| $t_S$ | Set-up Time, HIGH or LOW | 2.7 | 1.8 | 5.0 | 6.5 | ns |
| | | $3.3 \pm 0.3$ | 1.5 | 4.0 | 4.5 | |
| $t_H$ | Hold Time, HIGH or LOW | 2.7 | −2.4 | 0.5 | 0.5 | ns |
| | $D_n$ to $CP_n$ | $3.3 \pm 0.3$ | −2.0 | 0.5 | 0.5 | |
| $t_W$ | Pulse Width | 2.7 | 3.6 | 7.0 | 10.0 | ns |
| | | $3.3 \pm 0.3$ | 3.0 | 5.5 | 7.0 | |
| $t_{REC}$ | Recovery Time | 2.7 | −3.0 | 0 | 0 | ns |
| | | $3.3 \pm 0.3$ | −2.5 | 0 | 0 | |

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = Open |
| $C_{PD}$ (Note 10) | Power Dissipation Capacitance | 25 | pF | $V_{CC}$ = 3.3V |

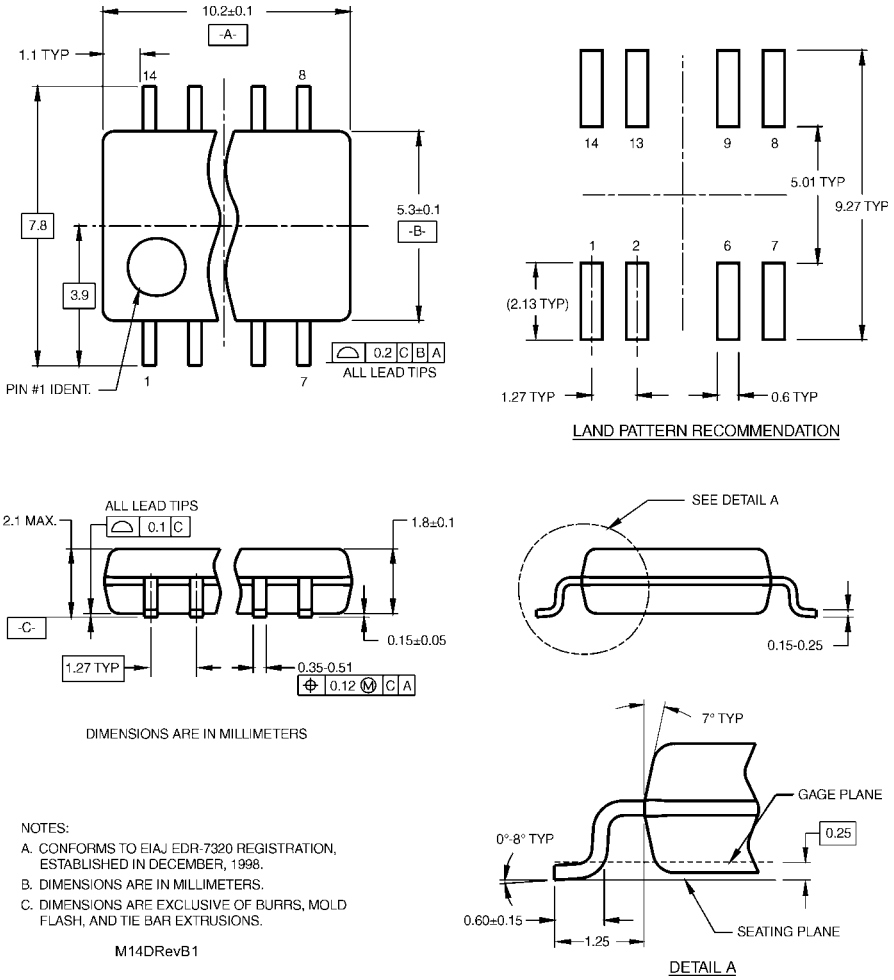
**Note 10:** $C_{PD}$ is measured at 10 MHz.

## Physical Dimensions inches (millimeters) unless otherwise noted




**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**
**Package Number M14A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M14D**



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